



AF/2816

AMENDMENT TRANSMITTAL LETTER

Docket No.
M4065.0176/P176

Application No. 09/354,302	Filing Date July 16, 1999	Examiner A. Luu	Art Unit 2816
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Applicant(s): Christopher K. Morzano

Invention: APPARATUS AND METHOD FOR ADJUSTING CLOCK SKEW

TO THE COMMISSIONER FOR PATENTS

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated and is transmitted as shown below.

CLAIMS AS AMENDED					
	Claims Remaining After Amendment	Highest Number Previously Paid	Number Extra Claims Present	Rate	
Total Claims	98	- 98 =		x	0.00
Independent Claims	10	- 10 =		x	0.00
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>					
Other fee (please specify):					
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT:					

Large Entity

Small Entity

No additional fee is required for this amendment.

Please charge Deposit Account No. _____ in the amount of \$ _____. A duplicate copy of this sheet is enclosed.

A check in the amount of \$ _____ to cover the filing fee is enclosed.

Payment by credit card. Form PTO-2038 is attached.

The Commissioner is hereby authorized to charge and credit Deposit Account No. 04-1073 as described below. A duplicate copy of this sheet is enclosed.

Credit any overpayment.

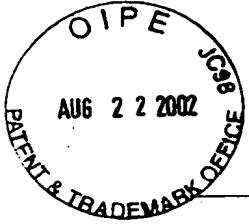
Charge any additional filing or application processing fees required under 37 CFR 1.16 and 1.17.

Dated: August 22, 2002

Thomas J. D'Amico

Attorney Reg. No.: 28,371

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 828-2232



PATENT
Docket No.: M4065.0176/P176

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Christopher Morzano

Serial No.: 09/354,302

Filed: July 16, 1999

Group Art Unit: 2816

Examiner: A. Luu

For: APPARATUS AND METHOD FOR
ADJUSTING CLOCK SKEW

Assistant Commissioner for Patents
Washington, D.C. 20231

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AMENDMENT

Dear Sir:

In response to the Final Office Action dated May 22, 2002 (Paper No. 15),
please amend the above-identified U.S. patent application as follows:

In the Claims:

1. (Twice Amended) A circuit for reducing clock signal skew comprising:
at least a first and second complementary clock signal input/output line for
receiving first and second complementary clock input signals and transmitting first and
second complementary clock output signals, wherein the complementary clock input
signals have a skewed time lag relative to each other;